What is claimed is:

1. A display device comprising:

a plurality of gate signal lines and

a plurality of pixels, each of said plurality of pixels controlled by at least one of said plurality of gate signal lines, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

switching of said TFT for erasing is controlled by voltage applied to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

switching of said first TFT for switching is controlled by voltage applied to a (k+1)th gate signal line of said plurality of gate signal lines;

switching of said second TFT for switching is controlled by voltage applied to a (k+2)th gate signal line of said plurality of gate signal lines;

a digital video signal is inputted to a gate electrode of said TFT for electroluminescence driving when both said first TFT for switching and said second TFT for switching are ON;

switching of said TFT for electroluminescence driving is controlled by said digital video signal;

said TFT for electroluminescence driving is turned off when said TFT for erasing is turned on; and

said electroluminescence element emits light when said TFT for electroluminescence driving is ON and does not emit light when said TFT for electroluminescence driving is off.

2. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines, wherein k is a natural number;

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving; and

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said electroluminescence element.

3. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines, (wherein k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+2)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving; and

a source region of said TFT for electroluminescence driving

is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said electroluminescence element.

4. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

said electroluminescence element comprises an anode, a cathode, and an electroluminescence layer provided between said anode and said cathode;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected

to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving;

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said anode; and said TFT for electroluminescence driving is a p-channel TFT.

5. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate

signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

said electroluminescence element comprises an anode, a cathode, and an electroluminescence layer provided between said anode and said cathode;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving;

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said cathode; and

said TFT for electroluminescence driving is an n-channel TFT.

6. A display device according to claim 4, wherein said electroluminescence layer is formed of a small molecular organic substance or a polymer organic material.

7. A display device according to claim 5, wherein said electroluminescence layer is formed of a small molecular organic substance or a polymer organic material.

8. A display device according to claim 6, wherein said small molecular organic material is formed of Alq_3 (tris-8-quinolinolate-aluminum) or a TPD (triphenylamine derivative).

9. A display device according to claim 7, wherein said small

molecular organic material is formed of Alq_3 (tris-8-quinolinolate-aluminum) or a TPD (triphenylamine derivative).

10. A display device according to claim 6, wherein said polymer organic material is formed of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), or polycarbonate.

11. A display device according to claim 7, wherein said polymer organic material is formed of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), or polycarbonate.

12. A display device according to claim 4, wherein:

said anode or cathode is connected directly or through at least one wiring to said drain region of said TFT for electroluminescence driving; and

a bank is formed over a region where said anode or cathode is connected to said drain region of said TFT for electroluminescence driving or to said at least one wiring.

13. A display device according to claim 5, wherein:

said anode or cathode is connected directly or through at least one wiring to said drain region of said TFT for electroluminescence driving; and

a bank is formed over a region where said anode or cathode is connected to said drain region of said TFT for electroluminescence driving or to said at least one wiring.

14. A display device according to claim 9, wherein said bank has a light blocking property.

15. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected

to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving;

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said electroluminescence element;

a plurality of writing periods Ta and a plurality of erasing periods Te are provided in one frame period;

said plurality of gate signal lines are sequentially selected according to a first selection signal sequentially inputted to said plurality of gate signal lines during said plurality of writing periods Ta;

said plurality of gate signal lines are serially selected

according to a second selection signal serially inputted to said plurality of gate signal lines during said plurality of erasing periods Te;

a period where a gate signal line is selected from said plurality of gate signal lines according to said first selection signal and a period where an adjacent gate signal line is selected overlap each other;

a period where a gate signal line is selected from said plurality of gate signal lines according to said second selection signal and a period where an adjacent gate signal line is selected do not overlap each other; and

a period where an arbitrary gate signal line is selected from said plurality of gate signal lines according to said first selection signal is twice as long as a period where said gate signal line is selected according to said second selection signal.

16. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for

switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving;

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and

a drain region of said TFT for electroluminescence driving is connected to said electroluminescence element;

a plurality of writing periods Ta and a plurality of erasing periods Te are provided in one frame period;

said plurality of gate signal lines are serially selected according to a first selection signal serially inputted to said plurality of gate signal lines during said plurality of writing periods Ta;

said plurality of gate signal lines are serially selected according to a second selection signal serially inputted to said plurality of gate signal lines during said plurality of erasing periods Te;

a period where a gate signal line is selected from said plurality of gate signal lines according to said first selection signal and a period where an adjacent gate signal line is selected overlap each other;

a period where a gate signal line is selected from said plurality of gate signal lines according to said second selection signal and a period where an adjacent gate signal line is selected do not overlap each other;

a digital video signal is inputted to said plurality of source signal lines during a period where said plurality of gate signal lines are selected according to said first selection signal; and

a period where an arbitrary gate signal line is selected from

said plurality of gate signal lines according to said first selection signal is twice as long as a period where said gate signal line is selected according to said second selection signal.

17. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal

lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving;

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said electroluminescence element;

n writing periods Ta1, Ta2, …, and Tan and (m-1) erasing periods Te1, Te2, …, and Te(m-1) are provided in one frame period (where m is an arbitrary number from 2 to n);

a digital video signal is inputted to said gate electrodes of said TFTs for electroluminescence driving during said writing periods Ta1, Ta2, …, and Tan;

said digital video signal inputted to said gate electrodes of said TFTs for electroluminescence driving is erased during said erasing periods Te1, Te2, …, and Te(m-1);

periods from the start of said writing periods Ta1, Ta2, …,

and Tan to the start of writing periods or erasing periods appearing subsequently to said writing periods Ta1, Ta2, …, and Tan are display periods Tr1, Tr2, …, and Tr(m-1), respectively;

periods from the start of said erasing periods Te1, Te2, …, and Te(m-1) to the start of writing periods appearing subsequently to said erasing periods Te1, Te2, …, and Te(m-1) are non-display periods Td1, Td2, …, and Tdn, respectively;

whether said electroluminescence elements emit light or not during said display periods Tr1, Tr2, …, and Trn is selected according to said digital video signal; and

ratio of lengths of said display periods Tr1, Tr2, …, and Trn is represented as $2^0 : 2^1 : \ldots : 2^{(n-1)}$.

18. A display device comprising:

a plurality of source signal lines;

a plurality of gate signal lines crossing said plurality of gate signal lines;

a plurality of power supply lines along said plurality of gate signal lines of said plurality of source signal lines; and

a plurality of pixels disposed in matrix-form, wherein:

each of said plurality of pixels comprises a first TFT for switching, a second TFT for switching, a TFT for erasing, a TFT for electroluminescence driving, and an electroluminescence element;

a gate electrode of said TFT for erasing is connected to a kth gate signal line of said plurality of gate signal lines (where k is a natural number);

a gate electrode of said first TFT for switching is connected to a (k+1)th gate signal line of said plurality of gate signal lines;

a gate electrode of said second TFT for switching is connected to a (k+2)th gate signal line of said plurality of gate signal lines;

one of a source region and a drain region of said second TFT for switching is connected to one of said plurality of source signal lines and the other is connected to a source region or a drain region of said first TFT for switching;

said source region or drain region of said first TFT for switching not connected to said source region or drain region of said second TFT for switching is connected to a gate electrode of said TFT for electroluminescence driving;

one of a source region and a drain region of said TFT for erasing is connected to one of said plurality of power supply lines and the other is connected to said gate electrode of said TFT for electroluminescence driving;

a source region of said TFT for electroluminescence driving is connected to one of said plurality of power supply lines and a drain region of said TFT for electroluminescence driving is connected to said electroluminescence element;

n writing periods Ta1, Ta2, ..., and Tan and (m-1) erasing periods

Te1, Te2, …, and Te(m-1) are provided in one frame period (where m is an arbitrary number from 2 to n);

a digital video signal is inputted to said gate electrodes of said TFTs for electroluminescence driving during said writing periods Ta1, Ta2, …, and Tan;

said digital video signal inputted to said gate electrodes of said TFTs for electroluminescence driving is erased during said erasing periods Te1, Te2, …, and Te(m-1);

periods from the start of said writing periods Ta1, Ta2, …, and Tan to the start of writing periods or erasing periods appearing subsequently to said writing periods Ta1, Ta2, …, and Tan are display periods Tr1, Tr2, …, and Tr(m-1), respectively;

periods from the start of said erasing periods Te1, Te2, …, and Te(m-1) to the start of writing periods appearing subsequently to said erasing periods Te1, Te2, …, and Te(m-1) are non-display periods Td1, Td2, …, and Tdn, respectively;

whether said electroluminescence elements emit light or not during said display periods Tr1, Tr2, …, and Trn is selected according to said digital video signal;

ratio of lengths of said display periods Tr1, Tr2, …, and Trn is represented as $2^0 : 2^1 : \ldots : 2^{(n-1)}$;

said plurality of gate signal lines are serially selected according to a first selection signal serially inputted to said plurality of gate signal lines during said writing periods Ta1,

Ta2, …, and Tan;

said plurality of gate signal lines are serially selected according to a second selection signal serially inputted to said plurality of gate signal lines during said erasing periods Te1, Te2, …, and Te(m-1);

a period where a gate signal line is selected from said plurality of gate signal lines according to said first selection signal and a period where an adjacent gate signal line is selected overlap each other;

a period where a gate signal line is selected from said plurality of gate signal lines according to said second selection signal and a period where an adjacent gate signal line is selected do not overlap each other; and

a period where an arbitrary gate signal line is selected from said plurality of gate signal lines according to said first selection signal is twice as long as a period where said gate signal line is selected according to said second selection signal.

19. A display device according to claim 17, wherein said display periods Tr1, Tr2, …, and Trn appear in random order.

20. A display device according to claim 18, wherein said display periods Tr1, Tr2, …, and Trn appear in random order.

21. A display device according to claim 17, wherein a longest non-display period among said non-display periods Td1, Td2, …, and Tdn appears last in one frame period.

22. A display device according to claim 18, wherein a longest non-display period among said non-display periods Td1, Td2, …, and Tdn appears last in one frame period.

23. A display device according to claim 15, wherein said plurality of writing periods Ta do not overlap each other.

24. A display device according to claim 16, wherein said plurality of writing periods Ta do not overlap each other.

25. A display device according to claim 17, wherein said writing periods Ta1, Ta2, …, and Tan do not overlap each other.

26. A display device according to claim 18, wherein said writing periods Ta1, Ta2, …, and Tan do not overlap each other.

27. A display device according to claim 15, wherein said plurality of erasing periods Te do not overlap each other.

28. A display device according to claim 16, wherein said

plurality of erasing periods Te do not overlap each other.

29. A display device according to claim 17, wherein said erasing periods Te1, Te2, …, and Te(m-1) do not overlap each other.

30. A display device according to claim 18, wherein said erasing periods Te1, Te2, …, and Te(m-1) do not overlap each other.

31. A display device according to claim 2, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

32. A display device according to claim 3, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching,

said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

33. A display device according to claim 4, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

34. A display device according to claim 5, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

35. A display device according to claim 15, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

36. A display device according to claim 16, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

37. A display device according to claim 17, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power

supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

38. A display device according to claim 18, further comprising:

gate wiring connected to said gate electrode of said TFT for electroluminescence driving; and

capacity wiring connected to one of said plurality of power supply lines,

wherein a gate insulating film of said first TFT for switching, said second TFT for switching, said TFT for erasing, and said TFT for electroluminescence driving is provided between said gate wiring and said capacity wiring.

39. A display device according to claim 2, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

40. A display device according to claim 3, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

41. A display device according to claim 4, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

42. A display device according to claim 5, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

43. A display device according to claim 15, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

44. A display device according to claim 16, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

45. A display device according to claim 17, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

46. A display device according to claim 18, wherein:

two of said plurality of pixels disposed along a direction of provision of said plurality of gate signal lines are adjacent to each other with sandwiching any one of said plurality of power supply lines therebetween and said respective source regions of said TFTs for electroluminescence driving of said two pixels are connected to said one of said plurality of power supply lines.

47. A display device according to claim 1, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

48. A display device according to claim 2, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

49. A display device according to claim 3, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

50. A display device according to claim 4, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

51. A display device according to claim 5, wherein said first

TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

52. A display device according to claim 15, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

53. A display device according to claim 16, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

54. A display device according to claim 17, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

55. A display device according to claim 18, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are n-channel TFTs.

56. A display device according to claim 1, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

57. A display device according to claim 2, wherein said first

TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

58. A display device according to claim 3, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

59. A display device according to claim 4, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

60. A display device according to claim 5, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

61. A display device according to claim 15, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

62. A display device according to claim 16, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

63. A display device according to claim 17, wherein said first

TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

64. A display device according to claim 18, wherein said first TFT for switching, said second TFT for switching, and said TFT for erasing are p-channel TFTs.

65. A display device according to claim 1, wherein said TFT for electroluminescence driving is driven in a linear region.

66. A display device according to claim 2, wherein said TFT for electroluminescence driving is driven in a linear region.

67. A display device according to claim 3, wherein said TFT for electroluminescence driving is driven in a linear region.

68. A display device according to claim 4, wherein said TFT for electroluminescence driving is driven in a linear region.

69. A display device according to claim 5, wherein said TFT for electroluminescence driving is driven in a linear region.

70. A display device according to claim 15, wherein said TFT for electroluminescence driving is driven in a linear region.

71. A display device according to claim 16, wherein said TFT for electroluminescence driving is driven in a linear region.

72. A display device according to claim 17, wherein said TFT for electroluminescence driving is driven in a linear region.

73. A display device according to claim 18, wherein said TFT for electroluminescence driving is driven in a linear region.

74. A display device according to claim 1, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

75. A display device according to claim 2, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

76. A display device according to claim 3, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

77. A display device according to claim 4, wherein said display device is a device selected from the group of consisting: a computer,

a video camera and a DVD player.

78. A display device according to claim 5, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

79. A display device according to claim 15, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

80. A display device according to claim 16, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

81. A display device according to claim 17, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.

82. A display device according to claim 18, wherein said display device is a device selected from the group of consisting: a computer, a video camera and a DVD player.